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UNITED STATES DISTRICT COURT

CENTRAL DISTRICT OF CALIFORNIA

SOUTHERN DIVISION

PROGRESSIVE SEMICONDUCTOR SOLUTIONS LLC, Plaintiff, v. QUALCOMM TECHNOLOGIES, INC. and MARVELL SEMICONDUCTOR, INC. Defendants.	CASE NO. **SACV13-01535 DMG (JEMx)** **COMPLAINT FOR INFRINGEMENT OF U.S. PATENT NOS. 6,473,349 AND 6,862,208** Jury Trial Demanded

Plaintiff PROGRESSIVE SEMICONDUCTOR SOLUTIONS LLC ("Plaintiff") files this Original Complaint against Defendants QUALCOMM TECHNOLOGIES, INC. and MARVELL SEMICONDUCTOR, INC. ("Defendants") alleging as follows:

I. THE PARTIES

1. PROGRESSIVE SEMICONDUCTOR SOLUTIONS LLC ("Plaintiff") is a Limited Liability Company organized and existing under the laws of the State of Texas, with a principal place of business in Plano, Texas.

2. Upon information and belief, Defendant QUALCOMM TECHNOLOGIES, INC. ("QUALCOMM") is a Delaware corporation with a principal place of business in San Diego, CA. Defendant QUALCOMM may be served with process by serving its Registered Agent, Corporation Service Company located at 2710 Gateway Oaks Drive, Suite 150N, Sacramento, CA 95833.

3. Upon information and belief, Defendant MARVELL SEMICONDUCTOR, INC. ("MARVELL") is a California corporation with a principal place of business in Santa Clara, CA. Defendant MARVELL may be served with process by serving its Registered Agent, CT Corporation System located at 818 West Seventh Street, Los Angeles, CA 90017.

II. JURISDICTION AND VENUE

4. This is an action for infringement of a United States patent. Federal question jurisdiction is conferred to this Court over such action under 28 U.S.C. §§ 1331 and 1338(a).

5. Upon information and belief, Defendants have had minimum contacts with the Southern Division of the Central District of California such that this venue is fair and reasonable. Defendants have committed such purposeful acts and/or transactions in this district that they reasonably should know and expect that they could be haled into this Court as a consequence of such activity. Upon information

and belief, Defendants have transacted and, at the time of the filing of this Complaint, are transacting business within the Southern Division of the Central District of California.

6. For these reasons, personal jurisdiction exists and venue is proper in this Court under 28 U.S.C. §§ 1391(b) and (c) and 28 U.S.C. § 1400(b).

III. PATENT INFRINGEMENT

7. On October 29, 2002, United States Patent No. 6,473,349 ("the '349 Patent") was duly and legally issued for "CASCODE SENSE AMP AND COLUMN SELECT CIRCUIT AND METHOD OF OPERATION." A true and correct copy of the '349 Patent is attached hereto as Exhibit "A" and made a part hereof.

8. On March 1, 2005, United States Patent No. 6,862,208 ("the '208 Patent") was duly and legally issued for "MEMORY DEVICE WITH SENSE AMPLIFIER AND SELF-TIMED LATCH." A true and correct copy of the '208 Patent is attached hereto as Exhibit "B" and made a part hereof.

9. The '349 and '208 Patents are referred to collectively as the "Patents-in-Suit."

10. By way of assignment, Plaintiff is the owner of all right, title and interest in and to the Patents-in-Suit, with all rights to enforce them against infringers and to collect damages for all relevant times, including the right to prosecute this action.

11. Upon information and belief, Defendants manufacture, make, have made, import, have imported, market, sell and/or use products and/or systems that infringe one or more claims of the Patents-in-Suit; and/or induce and/or contribute to the infringement of one or more of the claims of the Patents-in-Suit by others.

12. On information and belief, Defendant QUALCOMM, without authority, consent, right, or license, and in direct infringement of the Patents-in-Suit, manufactures, uses, sells, imports, and/or offers for sale systems and/or products

directly infringing one or more claims of the Patents-in-Suit. By way of example only, its MSM8960 chip directly infringes at least claim 1 of the '349 Patent, and at least claim 1 of the '208 Patent.

13. On information and belief, Defendant MARVELL, without authority, consent, right, or license, and in direct infringement of the Patents-in-Suit, manufactures, uses, sells, imports, and/or offers for sale systems and/or products directly infringing one or more claims of the Patents-in-Suit. By way of example only, its 88W8686 chip directly infringes at least claim 1 of the '349 Patent, and at least claim 1 of the '208 Patent.

14. Plaintiff reserves the right to assert additional claims of the Patents-in-Suit and reserves the right to assert additional patents.

15. Plaintiff has been damaged as a result of Defendants' infringing conduct. Defendants are, thus, liable to Plaintiff in an amount that adequately compensates for their infringement, which, by law, cannot be less than a reasonable royalty, together with interest and costs as fixed by this Court under 35 U.S.C. § 284.

16. Upon information and belief, Defendants will continue their infringement of the Patents-in-Suit unless enjoined by the Court. Defendants' infringing conduct has caused Plaintiff irreparable harm and will continue to cause such harm without the issuance of an injunction.

IV. PRAYER FOR RELIEF

WHEREFORE, Plaintiff respectfully requests that the Court find in its favor and against Defendants, and that the Court grant Plaintiff the following relief:

a. Judgment that one or more claims of the Patents-in-Suit have been infringed, either literally and/or under the doctrine of equivalents, by Defendants and/or by others to whose infringement Defendants have contributed to and/or by others whose infringement has been induced by Defendants;

b. Judgment that Defendants account for and pay to Plaintiff all damages to and costs incurred by Plaintiff because of Defendants' infringing activities and other conduct complained of herein;

c. That Defendants' infringement be found to be willful from the time Defendants became aware of the infringing nature of its services, which is the time of filing of Plaintiff's Complaint at the latest, and that the Court award treble damages for the period of such willful infringement pursuant to 35 U.S.C. § 284.

d. That Plaintiff be granted pre-judgment and post-judgment interest on the damages caused by Defendants' infringing activities and other conduct complained of herein;

e. That the Court declare this an exceptional case and award Plaintiff its reasonable attorney's fees and costs in accordance with 35 U.S.C. § 285;

f. That Defendants be permanently enjoined from any further activity or conduct that infringes one or more claims of the Patents-in-Suit; and

g. That Plaintiff be granted such other and further relief as the Court may deem just and proper under the circumstances.

DATED: September 30, 2013

BRANDON C. FERNALD
FERNALD LAW GROUP LLP

By: _____
Brandon C. Fernald
Attorneys for Plaintiff
PROGRESSIVE SEMICONDUCTOR SOLUTIONS LLC

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DEMAND FOR JURY TRIAL

Plaintiff respectfully demands a jury trial on all issues so triable pursuant to Fed. R. Civ. P. 38(b) and L.R. 38-1.

DATED: September 30, 2013

FERNALD LAW GROUP LLP
BRANDON C. FERNALD
RACHEL D. STANGER

By:_____
Brandon C. Fernald
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EXHIBIT A

US006473349B1

(12) **United States Patent**
Flannagan

(10) **Patent No.: US 6,473,349 B1**
(45) **Date of Patent: Oct. 29, 2002**

(54) **CASCODE SENSE AMP AND COLUMN SELECT CIRCUIT AND METHOD OF OPERATION**

(75) Inventor: **Stephen T. Flannagan**, Austin, TX (US)

(73) Assignee: **Motorola, Inc.**, Schaumburg, IL (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/997,330**

(22) Filed: **Nov. 29, 2001**

(51) **Int. Cl.**[7] **G11C 7/00**
(52) **U.S. Cl.** **365/205**; 365/207; 365/230.08
(58) **Field of Search** 365/205, 207, 365/203, 189.05, 230.08, 189.02; 327/51

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,658,160	A		4/1987	Young
4,677,592	A		6/1987	Sakurai et al.
4,796,230	A		1/1989	Young
4,888,503	A		12/1989	Young
5,023,841	A		6/1991	Akrout et al.
5,247,479	A		9/1993	Young
5,384,503	A		1/1995	Shu et al.
5,650,971	A	*	7/1997	Longway et al. 327/51
5,815,452	A		9/1998	Shen
6,327,203	B1	*	12/2001	Won 365/189.07

OTHER PUBLICATIONS

Evert Seevinck et al., "Current–Mode Techniques for High–Speed VLSI Circuits with Application to Current Sense Amplifier for CMOS SRAM's", 1991 IEEE journal of Solid–State Circuits, vol. 26, No. 4, Apr., 1991, pp. 525–536.

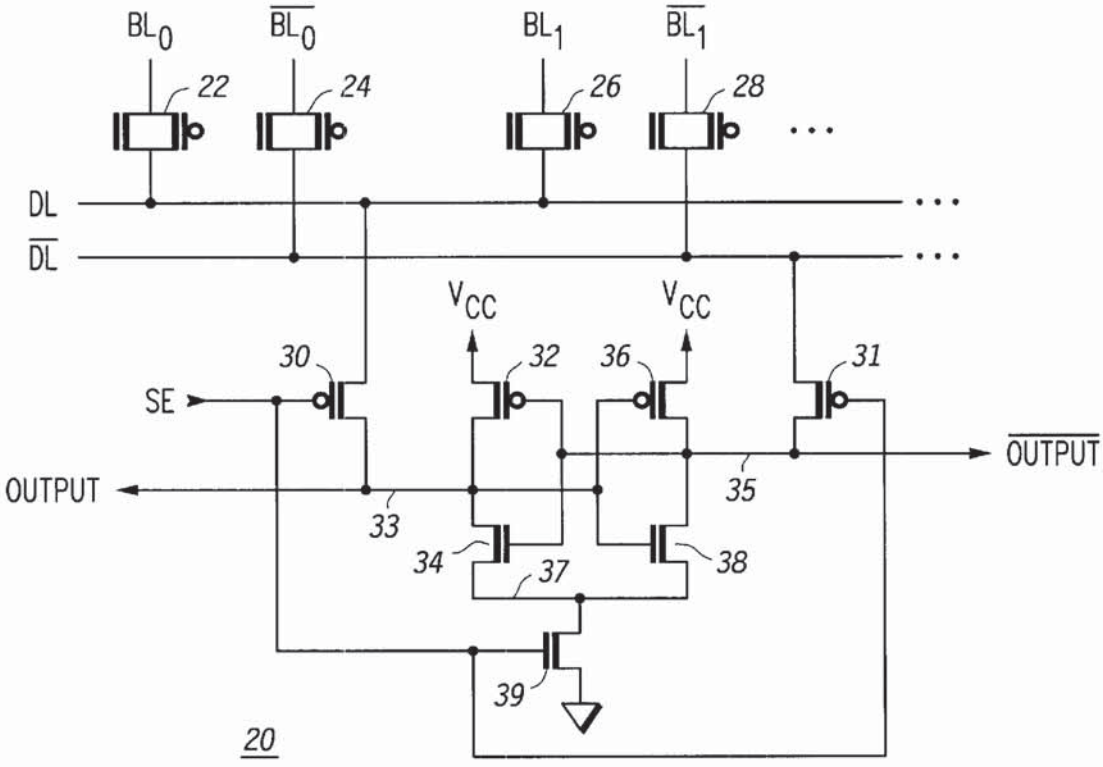
* cited by examiner

Primary Examiner—David Lam
(74) *Attorney, Agent, or Firm*—Robert L. King

(57) **ABSTRACT**

A sense amplifier uses a cascode stage (**76** or **100**) that receives a predetermined bit line pair differential signal and provides an output. The cascode stage output is coupled to a true and a complement output of the sense amplifier. In one form, a pair of pass transistors (**77**, **78**) and an amplifier (**79**) are coupled to the cascode stage and to complementary outputs and are controlled by a sense enable signal. The amplifier is operative only when the pair of pass transistors are made nonconductive. In another form, the cascode stage is connected directly to a bit line pair differential signal and to sense nodes (**82**, **86**) that are separately coupled to a data line pair by a coupler (**102**) and an amplifier (**104**).

17 Claims, 4 Drawing Sheets



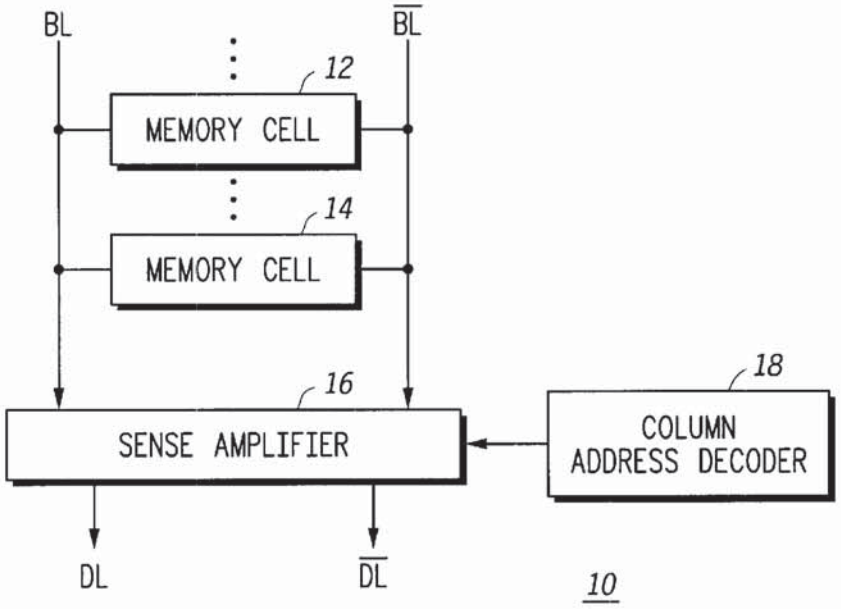

BL
$\overline{BL}$
12
MEMORY CELL
14
MEMORY CELL
16
SENSE AMPLIFIER
18
COLUMN ADDRESS DECODER
DL
$\overline{DL}$
10

FIG.1

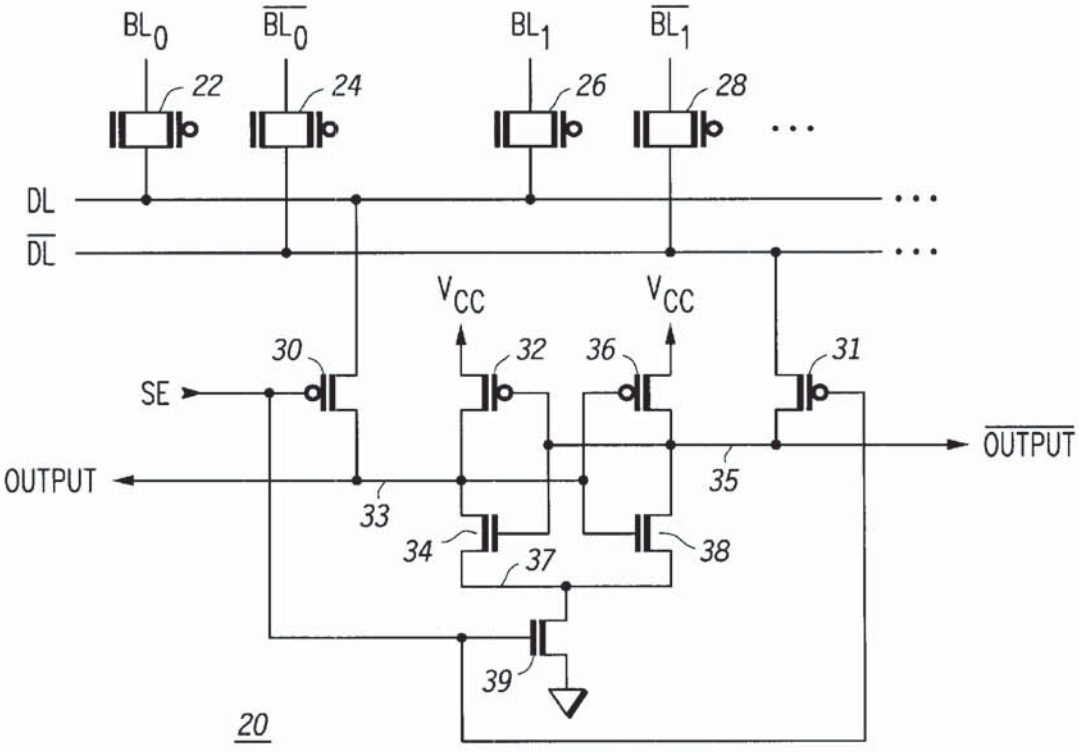

BL_0
$\overline{BL_0}$
BL_1
$\overline{BL_1}$
22
24
26
28
DL
$\overline{DL}$
V_{CC}
V_{CC}
30
32
36
31
SE
OUTPUT
$\overline{OUTPUT}$
33
35
34
37
38
39
20

FIG.2

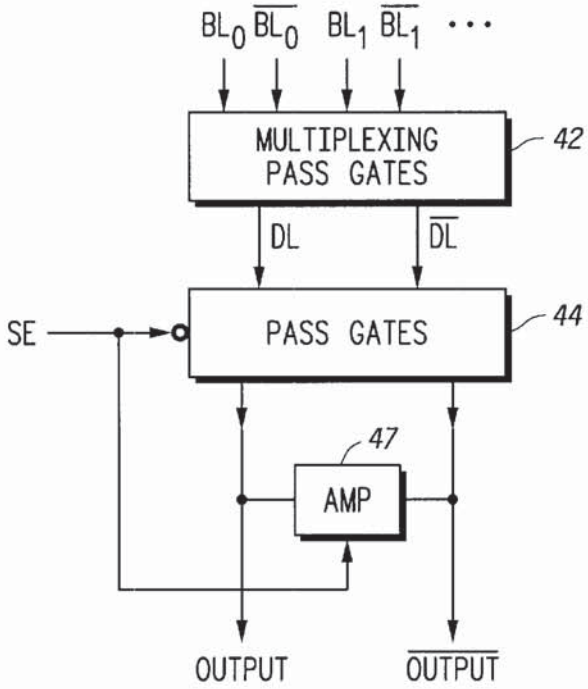

BL0 BL0 BL1 BL1 ...
MULTIPLEXING PASS GATES
42
DL
DL
SE
PASS GATES
44
47
AMP
OUTPUT
OUTPUT

FIG. 3

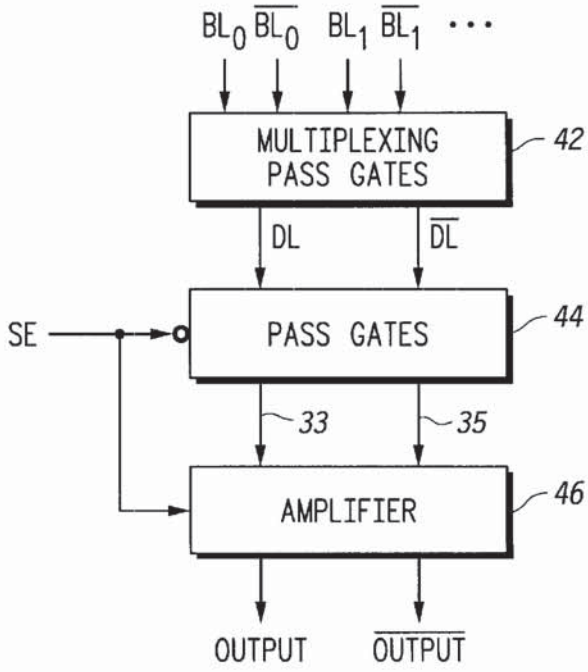

BL0 BL0 BL1 BL1 ...
MULTIPLEXING PASS GATES
42
DL
DL
SE
PASS GATES
44
33
35
AMPLIFIER
46
OUTPUT
OUTPUT

FIG. 4

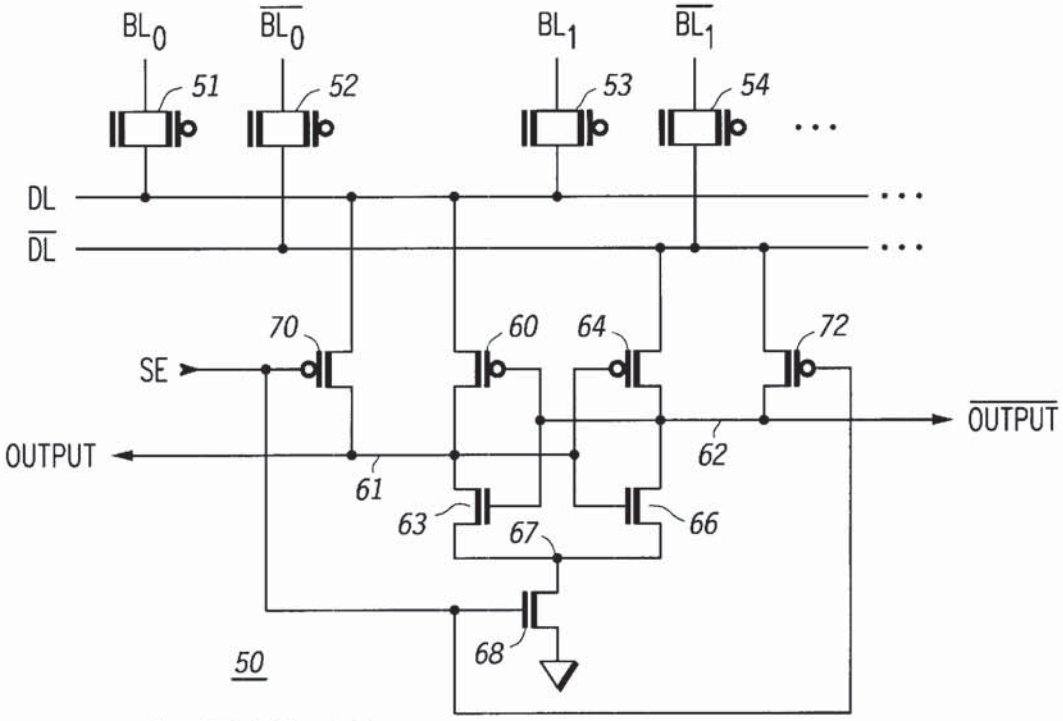

BL0
BL0
BL1
BL1
51
52
53
54
DL
DL
70
60
64
72
SE
OUTPUT
OUTPUT
61
62
63
66
67
68
50

FIG.5

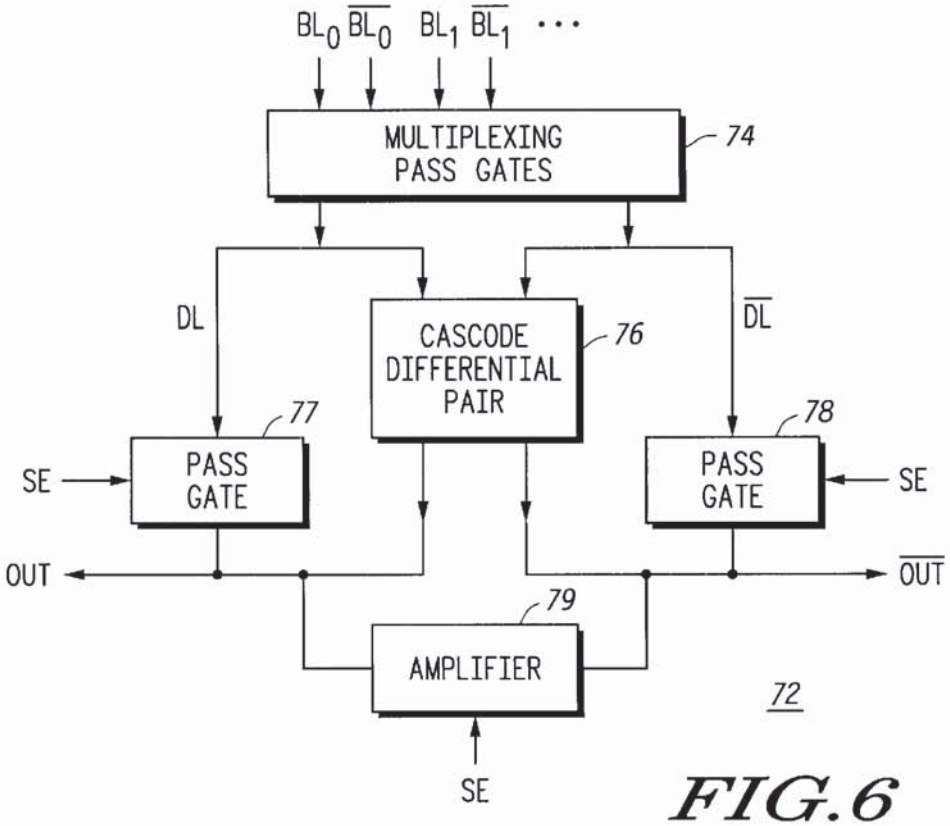

BL0 BL0 BL1 BL1
MULTIPLEXING PASS GATES
74
DL
CASCODE DIFFERENTIAL PAIR
76
DL
77
78
PASS GATE
PASS GATE
SE
SE
OUT
OUT
79
AMPLIFIER
72
SE

FIG.6

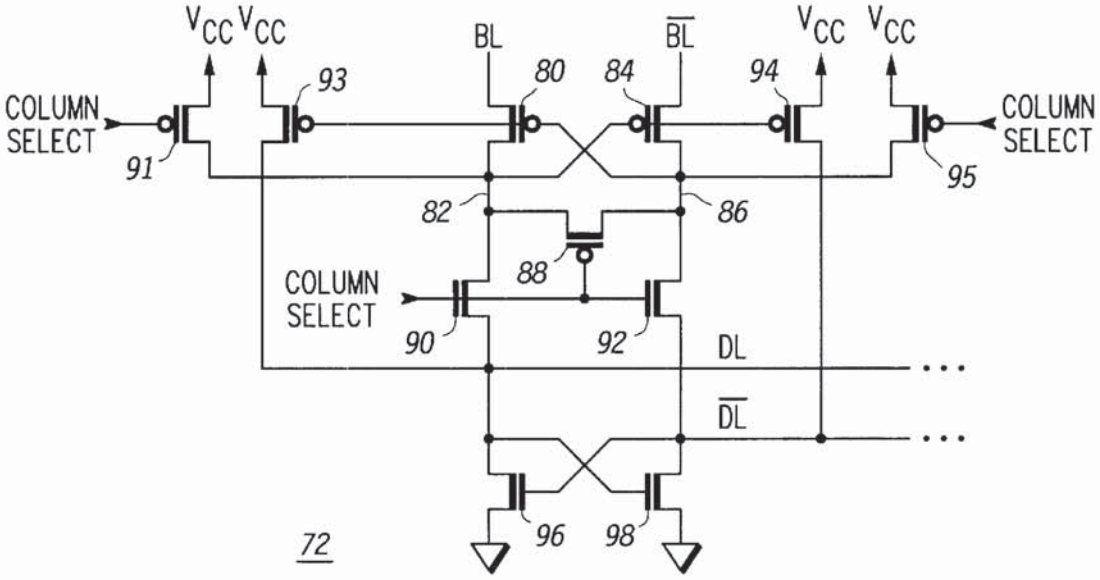

V_{CC} V_{CC}
BL
$\overline{BL}$
V_{CC} V_{CC}
COLUMN SELECT
93
80
84
94
COLUMN SELECT
91
95
82
86
88
COLUMN SELECT
90
92
DL
$\overline{DL}$
96
98
72

FIG. 7

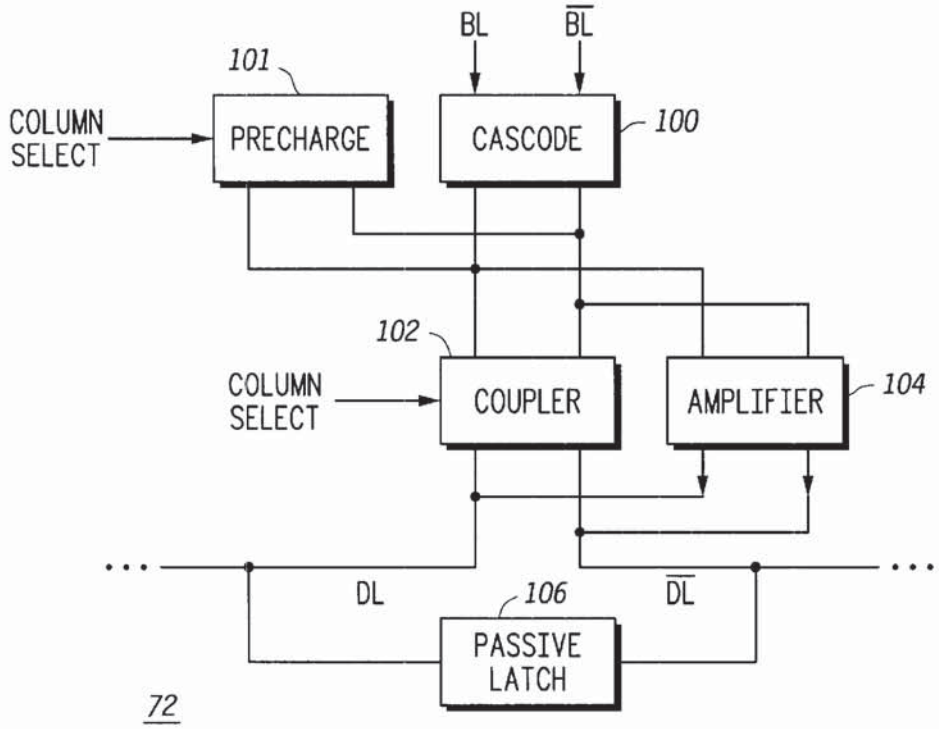

BL
$\overline{BL}$
101
COLUMN SELECT
PRECHARGE
CASCODE
100
102
COLUMN SELECT
COUPLER
AMPLIFIER
104
DL
106
$\overline{DL}$
PASSIVE LATCH
72

FIG. 8

CASCODE SENSE AMP AND COLUMN SELECT CIRCUIT AND METHOD OF OPERATION

FIELD OF THE INVENTION

This invention relates generally to semiconductor memories, and more specifically, to sense amplifiers used in semiconductor memories.

BACKGROUND OF THE INVENTION

Sense amplifiers are used in conjunction with memories such as a static random access memory array (SRAM). Sense amplifiers function to detect when complementary bit lines in a memory array exhibit a voltage transition in response to column and row decoding and a sense enable signal. In an SRAM, there is a need to amplify and decode signals provided via columns of memory cells. Transistor pass gates are frequently used to perform column decoding. However, the amplification and decoding of such signals needs to be done with minimized ohmic losses in transistor pass gates. A static RAM bit line differential bit line signal develops in a manner that increases with time. Hence, whenever a differential signal is conducted by a pass gate, there is detriment to the differential signal that may be characterized in terms of either a time delay or a reduction in its magnitude. In the art, these two characterizations are often referred to as an RC (resistance multiplied by capacitance) time delay or an RC delay. Pass devices for connecting bit lines to data lines tend to delay the passage of a differential signal due to the RC time constant. There is typically a trade between improving the timeliness or magnitude of bit line and data line signal levels versus device count and amplifier reliability. In general, amplifier reliability refers to the collective ability of all amplifiers in a memory to guarantee an accurate signal given known offsets and error voltages.

An objective of memory sense amplifiers is to avoid drawing excess charge from a bit line subsequent to clocking the sense amplifier. One technique to accomplish this objective is to use a cascode pair of transistors directly connected to the bit lines. A disadvantage of the cascode pair of transistors is that the cascode pair delivers a fairly small signal, as compared with the full V_{CC} power supply value, to the local data lines. As a result, driving a global data line with the small signal is problematic. Another technique to accomplish this objective is to turn off the column decoders subsequent to the clocking of the sense amplifier, and thereby avoid pulling current from the bit lines. This technique adds circuit complexity and timing criticality to the design.

It is desirable to sense a data signal with an amplifier containing a cross-differential coupled pair of transistors. The timing of turn-on of the sense amplifier is critical. One measure of a sense amplifier's quality is the minimum differential signal that the sense amplifier is able to accurately sense. An objective in sense amplifier design is to provide the maximum differential signal to the difference in gate-to-source drive (delta V_{GS}) of the differential cross-coupled pair. Another critical design parameter associated with sense amplifiers is associated with the operation of a differential cross-coupled pair of transistors. The design parameter involves insuring that the difference in gate-to-source drives is greater than zero at the time the pair is clocked. If not, the output signal may not be accurate. In general, prior sense amplifiers have involved a trade-off between speed, size and power consumption.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and is not limited by the accompanying figures, in which like references indicate similar elements.

FIG. **1** illustrates in partial schematic diagram form a memory having a sense amplifier for use with the present invention;

FIG. **2** illustrates in schematic diagram form of a sense amplifier in accordance with the present invention;

FIG. **3** illustrates in block diagram form a plan diagram of the sense amplifier of FIG. **2** using a first amplifier configuration;

FIG. **4** illustrates in block diagram form a plan diagram of the sense amplifier of FIG. **2** using a second amplifier configuration;

FIG. **5** illustrates in schematic diagram form another embodiment of a sense amplifier in accordance with the present invention;

FIG. **6** illustrates in block diagram form a plan diagram of the sense amplifier of FIG. **5**;

FIG. **7** illustrates in schematic diagram form yet another embodiment of the sense amplifier in accordance with the present invention; and

FIG. **8** illustrates in block diagram form a plan diagram of the sense amplifier of FIG. **7**.

Skilled artisans appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help improve the understanding of the embodiments of the present invention.

DETAILED DESCRIPTION

FIG. **1** illustrates a memory **10** in which the various embodiments of the sense amplifier disclosed herein may be utilized. The memory **10** has a plurality of memory cells, such as memory cell **12** and memory cell **14**. Each memory cell is connected between a bit line, BL, and a complementary bit line BL-bar. A predetermined memory cell is addressed using a row decoder (not shown) and the corresponding stored data value within the addressed memory cell is provided to a sense amplifier **16**. Sense amplifier **16** functions to amplify the signal value of the data and provide a corresponding data output via data line output DL and the complement data line DL-bar. A column address decoder **18** is connected to sense amplifier **16** and functions to select the column in which memory cells **12** and **14** reside in response to a column address. It should be appreciated that the column address decode action may be performed either upstream or downstream from the sense amplifier **16**, or it may alternatively be embodied within the sense amplifier **16**.

Illustrated in FIG. **2** is a sense amplifier **20** having a plurality of multiplexing pass gate pairs such as pass gates **22**, **24** and **26**, **28**, etc. Each pass gate pair has one pass gate connected to the data line, DL, and one pass gate connected to the complement data line, DL-bar. Pass gate **22** has a first terminal connected to bit line BL**0**, and a second terminal connected to the data line DL. Pass gate **24** has a first terminal connected to the complement bit line, BL**0**-bar, and a second terminal connected to the complement data line, DL-bar. Pass gate **26** has a first terminal connected to the bit line BL**1** and a second terminal connected to the data line DL. Pass gate **28** has a first terminal connected to the

complement bit line BL1 and a second terminal connected to the complement data line. For convenience of illustration, the control signals that are connected to true and complement control terminals of each of pass gates **22**, **24**, **26** and **28** are not illustrated and are conventional. It should be well understood that additional pass gates exist, but are not shown for convenience of illustration. In one form, a pass gate pair exists for each column in a memory in which sense amplifier **20** is used. A first terminal of a P-channel transistor pass gate **30** is connected to the data line DL. A control terminal of P-channel transistor pass gate **30** is connected to a Sense Enable signal, SE. A second terminal of P-channel transistor pass gate **30** is connected to an Output terminal at a node **33**. A source of a P-channel transistor **32** is connected to a power supply terminal V_{CC}. A drain of P-channel transistor **32** is connected to output terminal **33** and to a drain of an N-channel transistor **34**. A gate of P-channel transistor **32** is connected to a gate of N-channel transistor **34** at a node **35** that forms a complement Output terminal. A source of N-channel transistor **34** is connected to a node **37**. A source of a P-channel transistor **36** is connected to the V_{CC} power supply terminal. A drain of P-channel transistor **36** is connected to a drain of an N-channel transistor **38** at node **35**. A gate of P-channel transistor **36** is connected to a gate of N-channel transistor **38** at node **33**. A source of N-channel transistor **38** is connected to node **37**. A first terminal of a P-channel transistor pass gate **31** is connected to the complementary data line. P-channel transistor pass gate **31** has a control terminal connected to the Sense Enable signal and a second terminal connected to node **35**. An N-channel transistor **39** has a drain connected to node **37**, a gate connected to the Sense Enable signal, and a source connected to a ground terminal.

In operation, a signal from a memory cell (not shown) is applied to one of the bit line pairs, such as BL**0**, BL**0**-bar, etc. The multiplexing pass gates **22**, **24**, **26**, **28**, etc. can be turned on either before, during or after the information signal is applied to the bit line. The information signal then appears on the data line pair and is transmitted through pass gates **30** and **31** and arrives on nodes **33** and **35**, respectively. When the signal SE is asserted, pass gates **30** and **31** are turned off. Transistor **39** is turned on when signal SE is asserted. Because the transistor pair formed by transistors **34** and **38** is cross-coupled, transistors **34** and **38** respectively amplify the signal on nodes **33** and **35**. When the common mode level of nodes **33** and **35** is low enough, cross coupled P-channel transistors **32** and **36** begin amplifying in differential mode, further contributing to the amplification on nodes **33** and **35** and insuring full power supply voltage rail levels on nodes **33** and **35** which respectively form the outputs labeled OUTPUT and OUTPUT-bar. The timing of the assertion of signal SE in an active high form must come after an adequate differential signal has appeared on the data line pair, DL and DL-bar, and thereby also has appeared on nodes **33** and **35** through the conductivity of transistor pass gates **30** and **31**, respectively.

Illustrated in FIG. **3** is a plan view of sense amplifier **20** of FIG. **2** using a first amplifier configuration that is equivalent to the amplifier structure of FIG. **2**. In general, sense amplifier **20** may be considered to have a plurality of multiplexing pass gates **42**, a plurality of pass gates **44** and an amplifier **47**. The multiplexing pass gates **42** receive all of the bit lines at inputs thereof. Multiplexing pass gates **42** represent pass gates **22**, **24**, **26** and **28** of FIG. **2**. The multiplexing pass gates **42** function to multiplex the numerous bit lines and output a single data line and its complement. It should be appreciated that multiplexing pass gates **42** may be implemented as circuitry external to a sense amplifier. The pass gates **44** are represented in FIG. **2** by transistor pass gates **30** and **31**. The remaining circuitry in FIG. **2** forms amplifier **47** of FIG. **3**. It should be noted that the sense enable signal SE enables the pass gates **44** while disabling the amplifier **47**. Similarly, when sense enable signal SE activates amplifier **47**, pass gates **44** function to disconnect amplifier **47** from the data line pair.

Illustrated in FIG. **4** is another plan view of sense amplifier **20** of FIG. **2** using a second amplifier configuration, an amplifier **46**, which differs from the amplifier structure of FIG. **2**. For convenience of explanation, the same elements existing in FIGS. **2** and **3** are identically numbered. In contrast, in FIG. **4**, the outputs of pass gates **44** that correspond to nodes **33** and **35** of FIG. **2** are respectively connected to first and second inputs of amplifier **46**. Amplifier **46** differs from amplifier **47** of FIG. **3** in that amplifier **46** has first and second output terminals that are separate and distinct from the first and second input terminals. The first output terminal of amplifier **46** provides the true Output and the second output terminal of amplifier **46** provides the complement Output, Output-bar.

Illustrated in FIG. **5** is a sense amplifier **50** forming another embodiment of the present invention. A pass gate **51** has a first terminal connected to a bit line, BL**0**, and a second terminal connected to a data line, DL. A pass gate **52** has a first terminal connected to a complement bit line, BL**0**-bar, and a second terminal connected to a complement data line, DL-bar. A pass gate **53** has a first terminal connected to a bit line, BL**1**, and a second terminal connected to the DL line. A pass gate **54** has a first terminal connected to a complement bit line, BL**1** -bar, and a second terminal connected to the complement data line, DL-bar. Additional pass gates exist for additional columns, but are not shown for convenience. In one form, a pass gate pair exists for each column in the memory in which sense amplifier **50** is used. A source of a P-channel transistor **60** is connected to data line DL. Transistor **60** has a drain connected to a node **61** that forms an output terminal labeled "Output" and has a gate connected to a node **62** that forms a complement output terminal labeled "Output-bar". An N-channel transistor **63** has a drain connected to node **61**, a gate connected to node **62**, and a source connected to a node **67**. A P-channel transistor **64** has a source connected to the complement data line, DL-bar, a gate connected to node **61**, and a drain connected to node **62**. An N-channel transistor **66** has a drain connected to node **62**, a gate connected to node **61**, and a source connected to node **67**. An N-channel transistor **68** has a drain connected to node **67**, a gate connected to a Sense Enable signal, SE, and a source connected to a ground terminal that is one terminal of a power supply. A P-channel transistor pass gate **70** has a first terminal connected to the data line, DL, a control terminal connected to the Sense Enable signal, SE, and a second terminal connected to node **61**. A P-channel transistor pass gate **72** has a first terminal connected to the complement data line, DL-bar, a control terminal connected to the Sense Enable signal, SE, and a second terminal connected to node **62**.

In operation, a signal from a memory cell (not shown) is applied to one of the bit line pairs, such as BL**0**, BL**0**-bar, etc. The multiplexing pass gates **51**–**54**, etc. can be turned on either before, during or after the signal is applied to the bit line. The signal then appears on the data line pair and is transmitted through P-channel transistor pass gates **70** and **72** and arrives on nodes **61** and **62**, respectively, because the sense enable signal, SE, is inactive (i.e. a logic low). When the sense enable signal SE is asserted, P-channel transistor

pass gates **70** and **72** are turned off. N-channel transistor **68** is also made conductive. When N-channel transistor **68** becomes conductive, the cross-coupled pair of N-channel transistors **63**, **66** begin respectively amplifying the signal on nodes **61**, **62** in differential mode. When the common-mode level of nodes **61**, **62** is low enough, the pair of P-channel transistors **60** and **64** begins amplifying, in differential mode, the differential signal applied to their gates. Additional amplification is obtained in the pair of P-channel transistors **60** and **64** due to the data line pair differential signal being applied to their sources in a cascode manner.

As a result, the differential gate-to-source bias (delta Vgs) on the pair of P-channel transistors **60** and **64** is twice the magnitude of the differential signal on the data line DL and complementary data line, DL-bar. Thus, the pair of P-channel transistors **60** and **64** can tolerate twice the ordinary threshold voltage offset.

Illustrated in FIG. **6** is a plan view of sense amplifier **50** of FIG. **5** that summarizes generally sense amplifier **50**. Pass gates **51–54** may be generally represented as a plurality of multiplexing pass gates **74** for receiving the various bit line pairs in true and complement form. Again, in one form, the number of bit line pairs represents a number of columns of memory cells being addressed. Pass gates **74** function to multiplex the multiple bit line pairs and output a single bit line pair as data line, DL, and the complement data line, DL-bar. Transistors **70** and **72** may respectively be represented as a pass gate **77** and a pass gate **78** that respectively receive the data line and data line-bar inputs and selectively provide the data in response to the Sense Enable signal when in logic low form. Pass gates **77** and **78** respectively provide the data to output and output-bar terminals of amplifier **79** that also function as input terminals to amplifier **79**. In other words, the same terminals of amplifier **79** that are used as inputs are also used as outputs. Amplifier **79** of FIG. **6** corresponds to transistors **60**, **63**, **64**, **66** and **68** of FIG. **5**.

Illustrated in FIG. **7** is a sense amplifier **72** that represents another embodiment of the present invention. A P-channel transistor **80** has a source connected to a bit line, BL, a gate connected to a node **86**, and a drain connected to a node **82**. A P-channel transistor **84** has a source connected to a complement bit line, BL-bar, a gate connected to node **82**, and a drain connected to node **86**. A P-channel transistor **88** has a source connected to node **82**, a drain connected to node **86**, and a gate connected to a Column Select signal. An N-channel transistor **90** has a drain connected to node **82**, a gate connected to the Column Select signal, and a source connected to a data line, DL. An N-channel transistor **92** has a drain connected to node **86**, a gate connected to the Column Select signal, and a source connected to a complement data line, DL-bar. A P-channel transistor **93** has a source connected to a power supply terminal for receiving a supply voltage Vcc, a gate connected to the gate of P-channel transistor **80** and node **86**, and a drain connected to the data line DL. A P-channel transistor **94** has a source connected to the power supply terminal for receiving supply voltage Vcc, a gate connected to the gate of transistor **84** and node **82**, and a source connected to the complement data line, DL-bar. A P-channel transistor **91** has a source connected to the power supply terminal for receiving supply voltage Vcc, a gate connected to the Column Select signal and a drain connected to node **82**. A P-channel transistor **95** has a source connected to the power supply terminal for receiving supply voltage Vcc, a gate connected to the Column Select signal and a drain connected to node **86**. An N-channel transistor **96** has a drain connected to the data line DL, a gate connected to the complement data line, DL-bar, and a source connected to a ground terminal. An N-channel transistor **98** has a drain connected to the complement data line, DL-bar, a gate connected to the data line, DL, and a source connected to the ground terminal.

In operation, P-channel transistors **80** and **84** function as a cascode style cross-coupled pair of transistors that are connected directly to the bit line and complement bit line. The conduction of transistors **80** and **84** is dependent upon the voltage applied to their cross-coupled gates. It should be understood that for each bit line pair, the circuitry of FIG. **7**, except transistors **96** and **98**, is repeated. The sources of P-channel transistors **80** and **84** receive the differential signal. P-channel transistors **91** and **95** function as precharge devices to precharge the data line and data line-bar to a ground potential. P-channel transistors **91** and **95** are made conductive and couple the Vcc supply via N-channel transistors **90** and **92** to the gates of N-channel transistors **96** and **98** making each conductive. When the Column Select signal is inactive, transistor **88** is conductive and equalizes the voltage on each of nodes **82** and **86** that equally biases transistors **80** and **84**. The Column Select signal is then activated indicating that the column has been selected and making N-channel transistors **90** and **92** conductive. N-channel transistors **90** and **92** function as a coupler and provide current to the cross-coupled P-channel transistors **80** and **84**. Nodes **82**, **86** also provide the differential signal to P-channel transistors **93**, **94** that function to actively pull-up data lines DL and DL-bar, respectively. Transistors **96** and **98** function as a cross-coupled passive latch circuit that only operates when the data lines transition in voltage. Transistors **96** and **98** are not repeated for every column of the memory since they are connected to the data line and data line-bar. By the time transistors **96** and **98** become conductive, there is sufficient differential signal on the data line and data line-bar conductors to ensure that transistors **96** and **98** will not go the wrong way due to noise or offset. In other words, if there were not sufficient differential signal on the data line, noise or offset could incorrectly make one of transistor **96** or **98** first become conductive contrary to the eventual data value. In order to make sure that this circuit condition is met, DL and DL-bar must be precharged low in any of various ways, such as by using pre-charge transistors (not shown). Once either one of transistor **96** or **98** is first strongly conductive, the other transistor becomes non-conductive and the conduction will not change regardless of the data value. However, this potential problem is averted in the design of sense amplifier **72** because the switching action ensures that there is sufficient differential signal on the data line and data line-bar before transistors **96** and **98** become conductive. Transistors **96** and **98** are "helper" devices and do not bear the critical original signal as do transistors **80** and **84**. By the precharge function of transistors **91** and **95**, nodes **82** and **86** are precharged to Vcc.

In another form, the drains of transistors **93**, **94** may instead be connected respectively to nodes **82**, **86** rather than to the data line and data line-bar. The operation is similar but there is a slightly different functional effect in the voltage at the inputs (drain) of coupler N-channel transistors **90**, **92** and the data line and data line-bar.

Sense amplifier **72** drives the data line and data line-bar with both N-channel transistors **90**, **92** and P-channel transistors **93**, **94**. There is no ohmic loss across additional pass transistors involved in the column decode function. In other words, by placing the differential bit line signal at the sources of transistors **80** and **84**, the ohmic loss of passing the differential signal through a bit line/data line pass decode device is avoided. Further, sense amplifier **72** does not drain

current from either bit line after sensing. Therefore, there is not a critical timing issue for turning off sense amplifier **72**. Transistors **93** and **94** provide a full pull-up of the data lines DL, DL-bar, to Vcc. Sense amplifier **72** addresses speed, power and size issues without having an imbalance in any one of these design parameters with respect to the others. Typically, each of these parameters requires a circuit style that severely disadvantages the other design parameters.

Illustrated in FIG. **8** is a plan overview of sense amplifier **72** of FIG. **6**. In general, a cascode stage **100** receives a bit line pair, BL and BL-bar and has first and second outputs. A precharge portion **101** is controlled by a Column Select signal and is connected to the outputs of the cascode stage **100**. An amplifier **104** has first and second inputs respectively connected to the first and second outputs of the cascode stage **100**, and has first and second outputs respectively connected to the data line DL and complement data line, DL-Bar. A coupler **102** has first and second inputs respectively connected to the first and second outputs of the cascode stage **100**. Coupler **102** has first and second outputs respectively connected to the data line DL and complement data line, DL-bar. A passive latch **106** is connected to the data line DL and the complement data line, DL-bar.

In comparing sense amplifier **72** with the plan overview, the cascode stage is implemented by transistors **80** and **84**. The precharge portion **101** is implemented by transistors **91** and **95**. The amplifier **104** is implemented by transistors **93** and **94**. The coupler **102** is implemented by N-channel transistors **90** and **92**, and passive latch **106** is implemented by transistors **96** and **98**. It should be well understood that different circuitry than used in sense amplifier **72** may be substituted to implement the plan overview of FIG. **8**. For example, various amplifier structures may be used in lieu of the specific amplifier configuration illustrated.

By now it should be appreciated that there has been provided a sense amplifier that is fast, small in size and that is efficient in power consumption. By using gain elements in the form of transistors **80**, **84** that are connected to the bit line pairs prior to ohmic column selection gates, ohmic loss on the bit line is minimized. As a result, a stronger differential signal exists and this allows earlier and faster sensing to be accomplished. Additionally, the sense amplifier taught herein is able to obtain full resolution without continued current demand from the bit lines and thus power is conserved. Additionally, there are no timing critical signals associated with pass gates or the amplifier so that control circuitry is reduced and size minimized. By amplifying low-capacitance sense nodes, such as nodes **82** and **86** of FIG. **7**, to a full-rail potential, the sense amplifier provided herein is much more efficient than driving either data lines or global data lines, even when partial-level signals are used to drive such data lines. The sense amplifiers taught herein combine the function of column decoding with amplification. In a preferred form, N-channel transistors are used for the column select function to couple the differential signal to the data line pair. N-channel transistors have a higher gain than P-channel transistors. P-channel transistors are then used for the amplifier function to interface between the bit lines and the sense nodes, such as nodes **82**, **86** of FIG. **7**.

Because the apparatus implementing the present invention is, for the most part, composed of electronic components and circuits known to those skilled in the art, circuit details will not be explained in any greater extent than that considered necessary as illustrated above, for the understanding and appreciation of the underlying concepts of the present invention and in order not to obfuscate or distract from the teachings of the present invention.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. For example, various types of transistors, whether bipolar, MOS, GaAs or other may be used to implement the plan diagrams of the sense amplifier embodiments provided herein. Various amplifier structures may be used. Additionally, the sense amplifier may be used in various types of memories, such as SRAM, MRAM, etc. The sense amplifier may also be used with other data signals than with bit line pairs and data line pairs. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of the present invention.

Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all the claims. As used herein, the terms "comprises," "comprising," or any other variation thereof, are intended to cover a non-exclusive inclusion, such that a process, method, article, or apparatus that comprises a list of elements does not include only those elements but may include other elements not expressly listed or inherent to such process, method, article, or apparatus.

What is claimed is:

1. A sense amplifier comprising:

a pair of pass transistors having first and second inputs respectively connected to a data path and complementary data path for receiving a differential data signal, the pair of pass transistors respectively connecting the data path and complementary data path at first and second outputs thereof in response to a sense enable signal, the first and second inputs of the pair of pass transistors are not electrically the same as the first and second outputs thereof when the pair of pass transistors are disabled by the sense enable signal; and

an amplifier having a first input connected to the first output of the pair of pass transistors, a second input connected to the second output of the pair of pass transistors, and first and second outputs for providing sense amplifier data signals in complementary form, the amplifier being controlled by the sense enable signal and being operative only when the pair of pass transistors are made nonconductive by the sense enable signal.

2. The sense amplifier of claim **1** wherein the amplifier further comprises:

a first transistor of a first conductivity type having a first current electrode connected to a first power supply terminal, a control electrode connected to the first input of the amplifier, and a second electrode connected to the second input of the amplifier;

a second transistor of a second conductivity type having a first current electrode connected to the second current electrode of the first transistor, a control electrode connected to the first input of the amplifier, and a second current electrode;

a third transistor of the first conductivity type having a first current electrode connected to the first power supply terminal, a control electrode connected to the second input of the amplifier, and a second current electrode;

a fourth transistor of the second conductivity type having a first current electrode connected to the first input of the amplifier, a current electrode connected to the second input of the amplifier, and a second current electrode connected to the second current electrode of the second transistor; and

a fifth transistor of the second conductivity type having a first current electrode connected to the second current electrode of the second transistor and the second current electrode of the fourth transistor, a control electrode for receiving the sense enable signal, and a second current electrode connected to a second power supply terminal.

3. The sense amplifier of claim **1** wherein the amplifier further comprises:

a first transistor of a first conductivity type having a first current electrode connected to the data path, a second current electrode connected to the first output, and a control electrode connected to the second output;

a second transistor of a second conductivity type having a first current electrode connected to the second current electrode of the first transistor, a second current electrode, and a control electrode connected to the control electrode of the first transistor;

a third transistor of the first conductivity type having a first current electrode connected to the complementary data path, a second current electrode connected to the second output, and a control electrode connected to first output;

a fourth transistor of the second conductivity type having a first current electrode connected to the second current electrode of the third transistor, a second current electrode connected to the second current electrode of the second transistor, and a control electrode connected to the first output; and

a fifth transistor of the second conductivity type having a first current electrode connected to the second current electrode of both the second transistor and the fourth transistor, a control electrode for receiving the sense enable signal, and a second current electrode connected to a power supply terminal.

4. The sense amplifier of claim **1** further comprising:

a plurality of transistor pass gate pairs, each of the plurality of transistor pass gate pairs having first and second inputs respectively connected to a predetermined bit line and complementary bit line pair of a memory and first and second outputs respectively connected to a memory data path and complementary memory data path.

5. The sense amplifier of claim **4** wherein the plurality of transistor pass gate pairs equals a number of columns in the memory.

6. The sense amplifier of claim **1** wherein the data path is a memory bit line.

7. The sense amplifier of claim **1** wherein the data path is a memory data line.

8. A sense amplifier comprising:

a pair of pass transistors having first and second inputs respectively connected to a data path and complementary data path for receiving a differential data signal, the pair of pass transistors respectively connecting the data path and complementary data path at first and second outputs thereof in response to a sense enable signal; and

an amplifier having a first input connected to the first output of the pair of pass transistors, a second input connected to the second output of the pair of pass transistors, and first and second outputs for providing sense amplifier data signals in complementary form, the amplifier being controlled by the sense enable signal and being operative only when the pair of pass transistors are made nonconductive by the sense enable signal, wherein the first output and the second output of the amplifier are electrically the same as the first input and the second input of the amplifier, respectively.

9. A sense amplifier comprising:

a cascode stage having a first input connected to a first data path, a second input connected to a first complementary data path, an output connected to a second data path, and a complementary output connected to a second complementary data path;

a coupler having a first pair of current electrodes connected to the second data path and second complementary data path, a control electrode, and a second pair of current electrodes connected to a third data path and a third complementary data path; and

a latch having a first input connected to the third data path, a second input connected to the third complementary data path, a control input connected to the third data path a complementary control input connected to the third complementary data path.

10. The sense amplifier of claim **9** further comprising:

an amplifier having a true input connected to the second data path, a complement input connected to the second complementary data path, a true output connected to a third data path, and a complement output connected to the third complementary data path.

11. The sense amplifier of claim **9** further comprising:

a precharge means connected to the second data path and the second complementary data path for selectively biasing the cascode stage in a nonconductive state in response to a control signal to thereby electrically isolate the first data path and the first complementary data path from the sense amplifier.

12. The sense amplifier of claim **9**, wherein the cascode stage further comprises:

a cascode pair of transistors having a first transistor of a first conductivity type having a first current electrode connected to a first data path, a control electrode, and a second current electrode connected to a second data path, and having a second transistor of the first conductivity type having a first current electrode connected to a first complementary data path, a control electrode connected to the second current electrode of the first transistor, and a second current electrode connected to the control electrode of the first transistor and to a second complementary data path.

13. A method of sensing a differential signal on a pair of input conductors, comprising:

receiving the differential signal;

using a pair of pass transistors to connect the pair of input conductors to a first output and a second output in response to a sense enable signal, a first of the pair of pass transistors having an input connected to a first signal of the differential signal and electrically connecting the first signal to the first output in response to the sense enable signal, a second of the pair of pass transistors having an input connected to a second signal of the differential signal and electrically connecting the second signal to the second output in response to the sense enable signal; and

coupling a first input of an amplifier to the first output and coupling a second input of the amplifier to the second

output, and coupling first and second outputs of the amplifier to a data line pair of conductors, the amplifier being controlled by the sense enable signal and being operative only when the pair of pass transistors are made nonconductive by the sense enable signal.

14. A sense amplifier comprising:

a first transistor of a first conductivity type having a first current electrode connected to a bit line, a control electrode, and a second current electrode;

a second transistor of the first conductivity type having a first current electrode connected to a complement of the bit line, a control electrode connected to the second current electrode of the first transistor, and a second current electrode connected to the control electrode of the first transistor;

a third transistor of a second conductivity type having a first current electrode connected to the second current electrode of the first transistor, a control electrode for receiving a column select signal, and a second current electrode for providing a first output of the sense amplifier;

a fourth transistor of the second conductivity type having a first current electrode connected to the second current electrode of the second transistor, a control electrode for receiving the column select signal, and a second current electrode for providing a second output of the sense amplifier;

a fifth transistor of the second conductivity type having a first current electrode connected to the second current electrode of the third transistor, a control electrode connected to the second current electrode of the fourth transistor, and a second current electrode connected to a reference voltage terminal; and

a sixth transistor of the second conductivity type having a first current electrode connected to the second current electrode of the fourth transistor, a control electrode connected to the second current electrode of the third transistor, and a second current electrode connected to the reference voltage terminal.

15. The sense amplifier of claim **14** further comprising:

a seventh transistor of the first conductivity type having a first current electrode connected to a second reference voltage terminal, a control electrode connected to the control electrode of the first transistor, and a second current electrode connected to the second current electrode of the third transistor; and

an eighth transistor of the first conductivity type having a first current electrode connected to the second reference voltage terminal, a control electrode connected to the control electrode of the second transistor, and a second current electrode connected to the second current electrode of the fourth transistor, the seventh transistor and the eighth transistor selectively amplifying the first output and the second output of the sense amplifier.

16. The sense amplifier of claim **15** further comprising:

a precharge means connected to the control electrode of each of the first transistor and the second transistor for selectively biasing the first transistor and the second transistor in a nonconductive state in response to the column select signal to thereby electrically isolate the bit line and the complement bit line from the sense amplifier.

17. The sense amplifier of claim **16** further comprising:

an equalization transistor of the first conductivity type having a first current electrode connected to the second current electrode of the first transistor, a second current electrode connected to the second current electrode of the second transistor, and a control electrode connected to the column select signal.

* * * * *

EXHIBIT B

US006862208B2

(12) **United States Patent**
Palmer et al.

(10) **Patent No.: US 6,862,208 B2**
(45) **Date of Patent: Mar. 1, 2005**

(54) **MEMORY DEVICE WITH SENSE AMPLIFIER AND SELF-TIMED LATCH**

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(73) Assignee: **Freescale Semiconductor, Inc.**, Austin, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(22) Filed: **Apr. 11, 2003**

(65) **Prior Publication Data**

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(51) **Int. Cl.**[7] **G11C 11/00**
(52) **U.S. Cl.** **365/154**; 365/205
(58) **Field of Search** 365/145, 222, 365/205, 154

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,701,268 A * 12/1997 Lee et al. 365/205
6,101,145 A 8/2000 Nicholes 365/230.01
6,445,632 B2 * 9/2002 Sakamoto 365/205

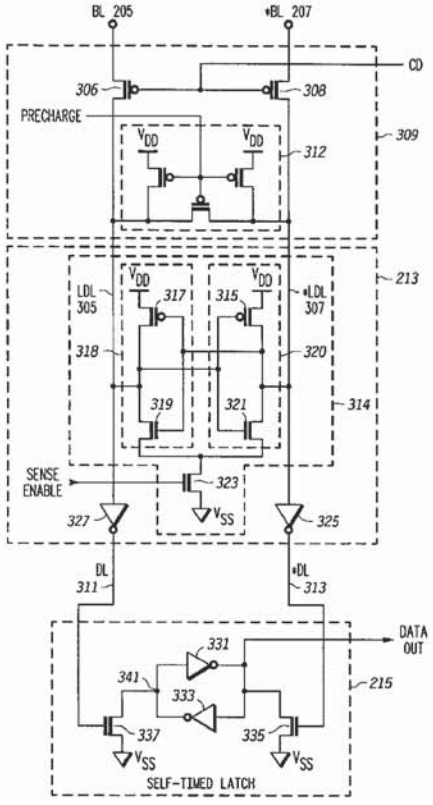
* cited by examiner

Primary Examiner—M. Tran
(74) *Attorney, Agent, or Firm*—David G. Dolezal; Daniel D. Hill

(57) **ABSTRACT**

A memory device **(201)** includes a plurality of memory cells **(203)**, bit lines, word lines, a sense amplifier **(314)**, and a self-timed latch **(215)**. The sense amplifier **(314)**, responsive to a sense enable signal, is for sensing and amplifying a voltage on the bit lines corresponding to a stored logic state of a selected one of the plurality of memory cells. An isolation circuit **(306, 308)** is coupled between the bit lines **(205** and **207)** and the sense amplifier **(314)**. The isolation circuit **(306, 308)** is for decoupling the selected one of the plurality of memory cells from the sense amplifier **(314)** at about the same time that the sense enable signal is asserted. A self-timed latch **(215)** is coupled to the sense amplifier **(314)**. The self-timed latch **(215)** does not receive a clock signal and is responsive to only the amplified voltage.

32 Claims, 4 Drawing Sheets



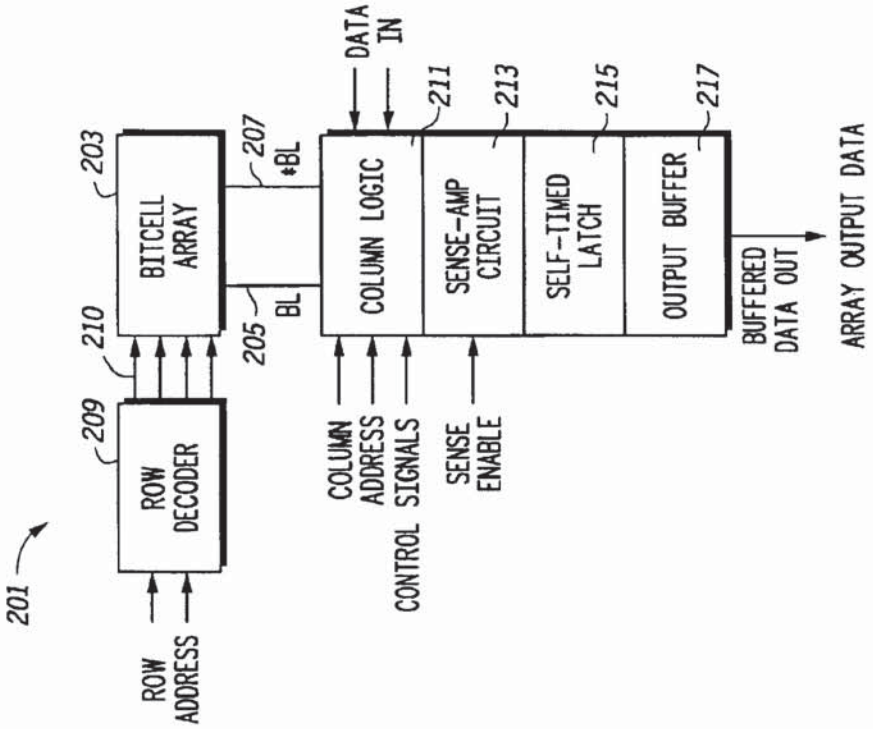


FIG.2

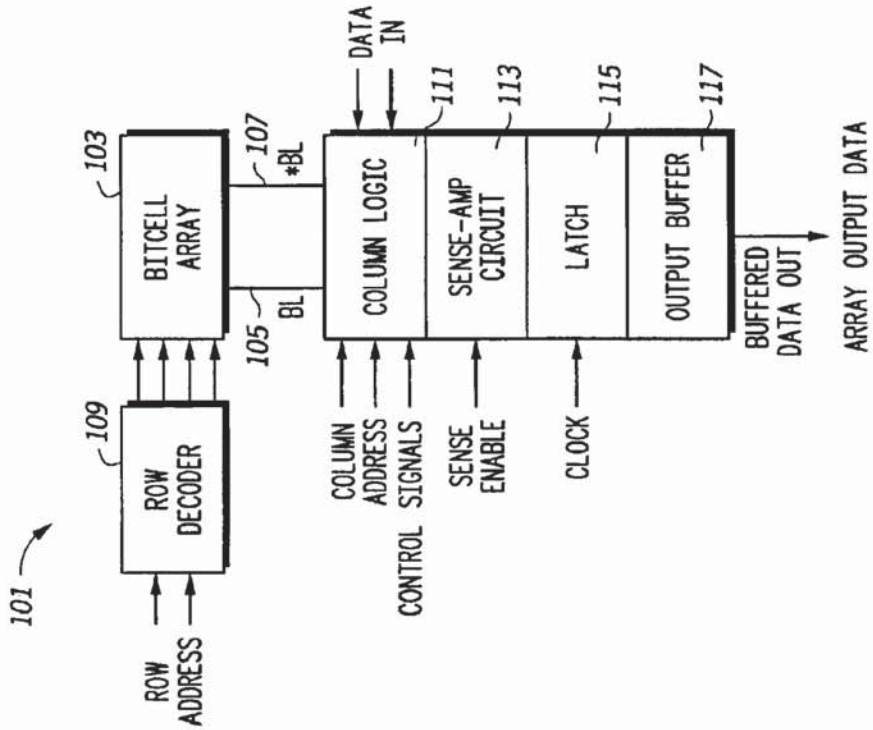
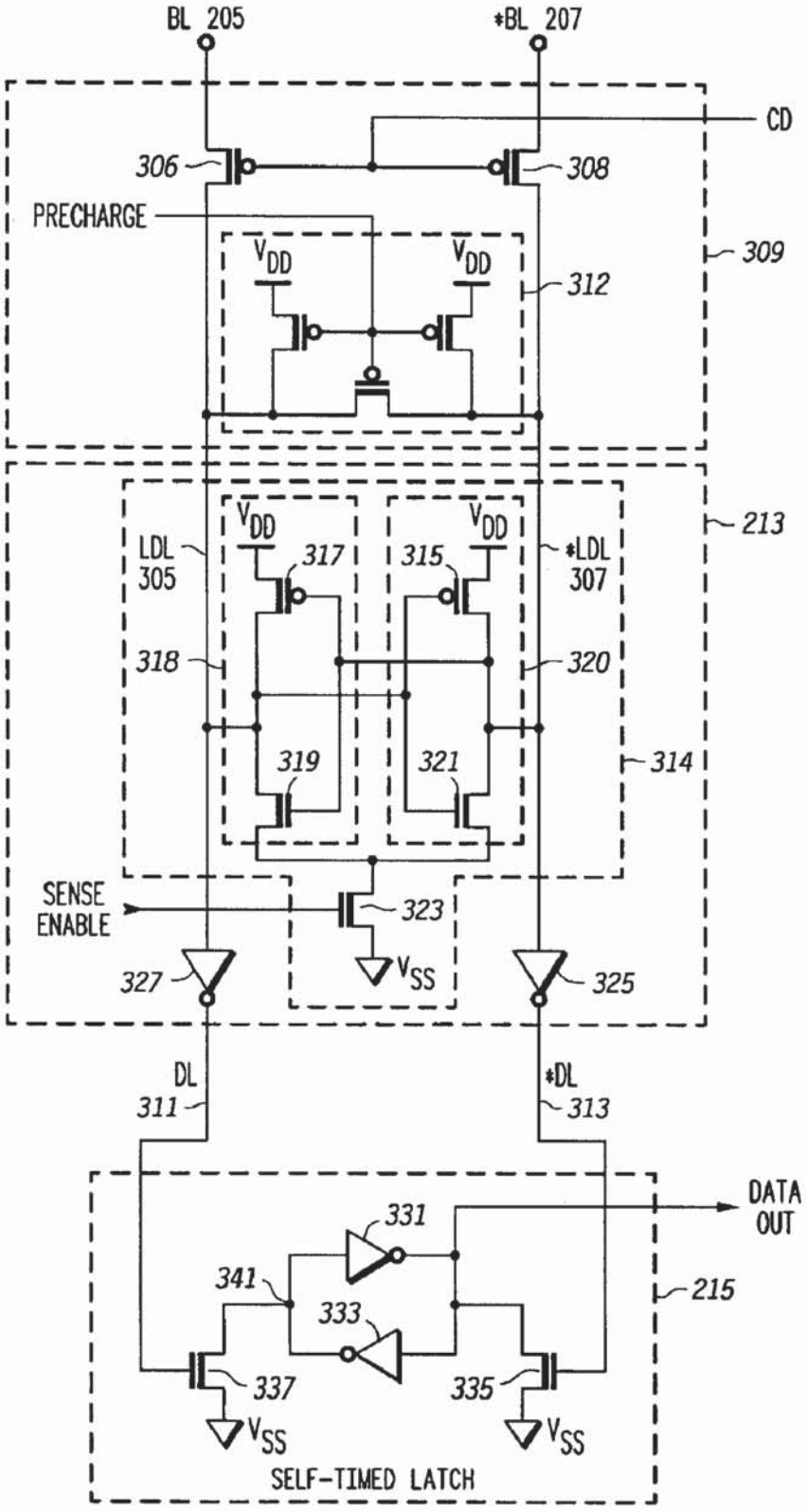


FIG.1
-PRIOR ART-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319
321
314
SENSE ENABLE
323
V_{SS}
327
325
DL 311
*DL 313
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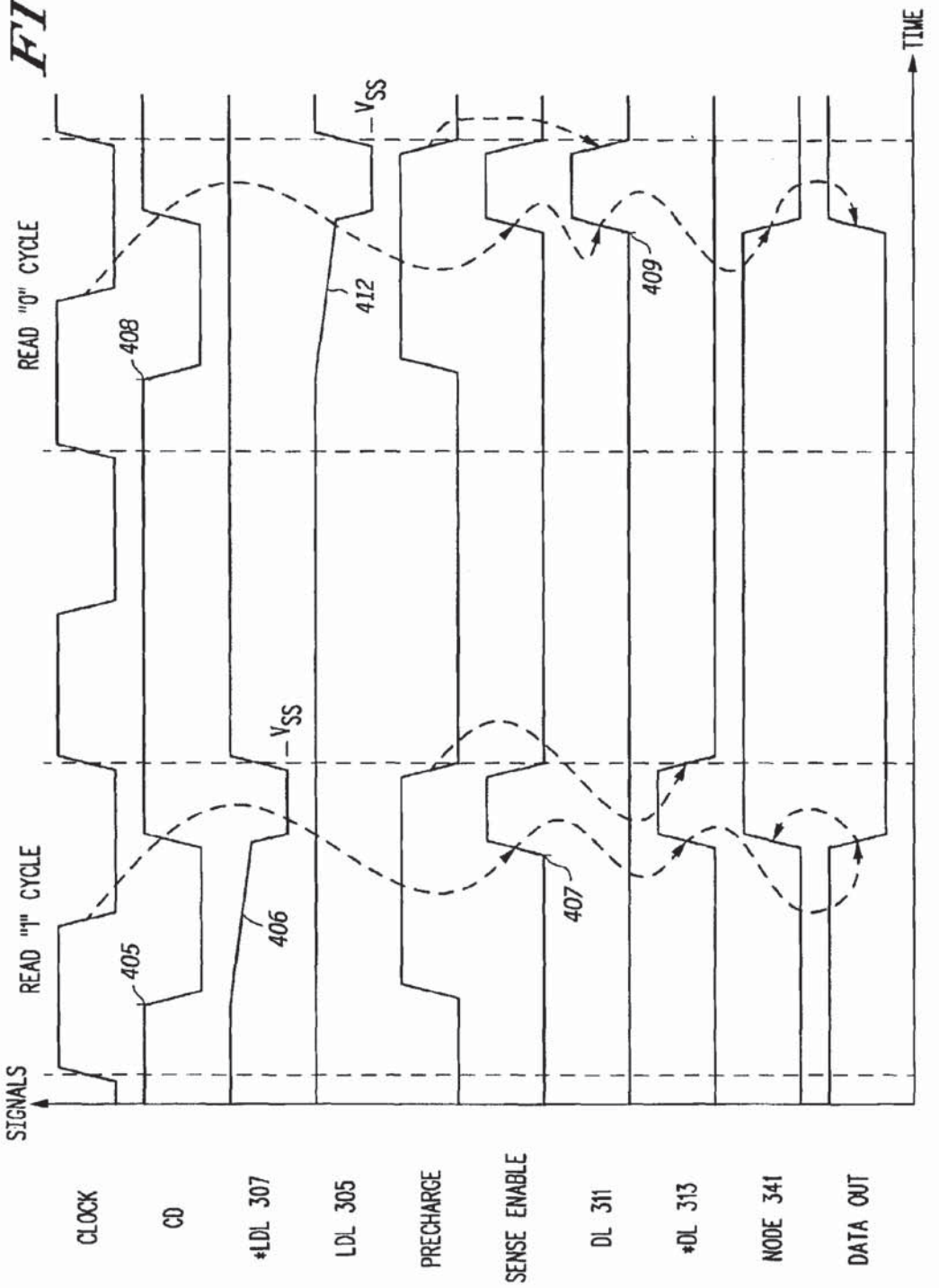
V_{SS}
SELF-TIMED LATCH

FIG.3

FIG. 4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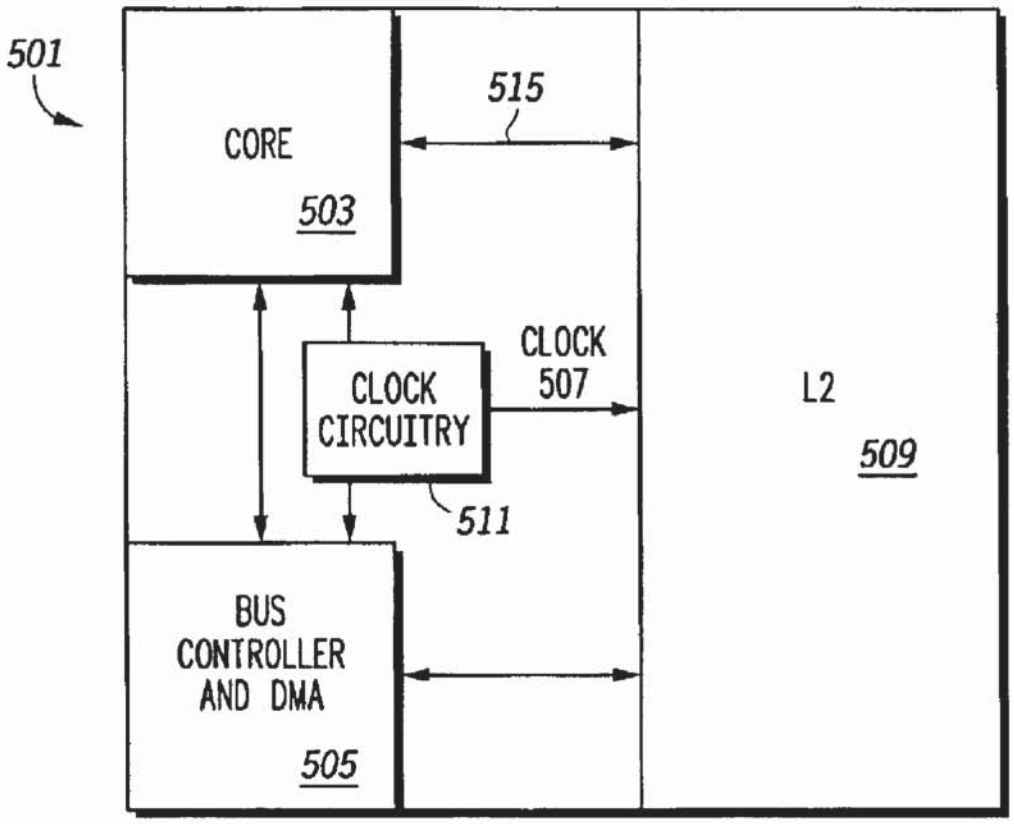
501
515
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CLOCK
507
CLOCK
CIRCUITRY
511
L2
509
BUS
CONTROLLER
AND DMA
505

FIG. 5

MEMORY DEVICE WITH SENSE AMPLIFIER AND SELF-TIMED LATCH

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates in general to integrated circuits and in particular to memory devices.

2. Description of the Related Art

Memory devices such as e.g. a Random Access Memory (RAM) include sense amplifiers for providing a signal indicative of a value stored in a memory cell of an array coupled to the sense amplifier.

FIG. **1** shows a prior art memory device. Memory device **101** includes a bitcell array **103** having a plurality of memory cells, each for storing a bit of data. The memory cells of bitcell array **103** are each coupled to a pair of differential bit lines BL **105** and *BL **107**. Each cell in array **103** is coupled to a word line, which is coupled to row decoder **109**. Memory device **101** also includes a column logic **111**, sense amplifier circuit **113**, latch **115**, and output buffer **117**. Column logic **111** includes precharge and equalization circuitry, write circuitry, column decode circuitry, and isolation transistors. Latch **115** receives a capacity CLOCK timing signal for enabling latch **115** to sample data from the output of sense amplifier circuit **113**. The second amplifier circuit **113** is enabled by a SENSE ENABLE signal.

For memory devices having multiple sense amplifier circuits and latches, providing a clock signal to each latch places a large load on a clock generating circuit, thereby consuming power and degradating the performance of the clock signal. Furthermore, enabling latch **115** with a clock signal requires specific setup and hold time requirements to be maintained between the clock signal and the sense enable signal. Variation in the performance of the memory device may result in the failure to latch the output of the sense amplifier circuit **113**. In addition, a latch requires extra circuitry to handle the clock signal. Furthermore, having a latch circuit with a clock input may also introduce unnecessary delay in the operation of a memory device.

What is needed is an improved memory device.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

FIG. **1** is a block diagram of a prior art memory device.

FIG. **2** is a block diagram of one embodiment of a memory device according to the present invention.

FIG. **3** is circuit diagram of one embodiment of a portion of the memory device of FIG. **2**, including the sense amplifier circuit and self-timed latch according to the present invention.

FIG. **4** is a timing diagram for one embodiment of a memory device according to the present invention.

FIG. **5** is a block diagram of one embodiment of an integrated circuit according to the present invention.

The use of the same reference symbols in different drawings indicates identical items unless otherwise noted.

DETAILED DESCRIPTION

The following sets forth a detailed description of a mode for carrying out the invention. The description is intended to be illustrative of the invention and should not be taken to be limiting.

FIG. **2** is a block diagram of a memory device according to the present invention. Memory device **201** includes a bitcell array **203** having a plurality of memory cells, each for storing a bit of data. In one embodiment, memory device **201** is an SRAM memory and the memory cells of bitcell array **203** are 6 transistor SRAM cells. However in other embodiments, other types of memory cells may be utilized in a memory device such as, e.g., other types of SRAM, DRAM, MRAM, Flash Memory, ROM, EPROM, EEPROM, ferromagnetic, or other types of memory cells. In some embodiments, each cell in bitcell array **203** stores multiple bits. The memory cells of bitcell array **203** are each coupled to a pair of differential bit lines BL **205** and *BL **207**. Each cell in array **203** is coupled to a word line (e.g. **210**), which are controlled by row decoder **209**. Row decoder **209** receives at its input, a row address which it decodes to assert the word line designated by the row address. Memory device **201** also includes column logic **211**. In one embodiment, column logic includes precharge and equalization circuitry, write circuitry, column decode circuitry, and isolation transistors (e.g. **306** and **308** in FIG. **3**). The column logic has inputs coupled to column address lines and coupled to data in lines for data writes to the memory cells. In some embodiments, column logic **211** may also be coupled to multiple pairs of bit lines, wherein column logic **211** performs a column decode function in coupling a selected column to sense amplifier circuit **213**.

Sense amplifier circuit **213** amplifies a difference in local data lines (e.g. LDL **305** and *LDL **307** in FIG. **3**) during a read cycle for the determination of the value of a bit stored in a memory element of a memory cell of bitcell array **203**. The value of a bit stored in a memory element corresponds to the logic state of the memory element. Sense amplifier circuit **213** is enabled to amplify a difference in the local data lines by a SENSE ENABLE signal.

Memory device **201** includes a self-timed latch **215**. Self-timed latch **215** is a data storage device that stores data provided from the sense amplifier circuit **213**. In one embodiment, self-timed latch **215** stores data only in response to receiving an amplified differential data signal from sense amplifier circuit **213**. Self-timed latch **215** does not have an input for a clock signal. The output of self-timed latch **215** is provided to an output buffer which provides a buffered data output signal indicating the value of the bit stored in the selected memory cell.

FIG. **3** is a schematic diagram showing one embodiment of sense amplifier circuit **213**, self-timed latch **215**, and a portion **309** of column logic **211** (hereafter "circuit portion **309**"). Circuit portion **309** includes two isolation transistors **306** and **308** for isolating bit lines BL **205** and *BL **207** from sense amplifier circuit **213**. The "*" in front of a signal line indicates that that signal line is a logical complement of the signal line having the same name but without the "*". Isolation transistors **306** and **308** are controlled by an isolation control signal (CD). In one embodiment, the isolation control signal (CD) is provided by a column decoder (not shown) of the column logic **211** and is a decoded signal from the column address provided to column logic **211**. Circuit portion **309** also includes a precharge and equalization circuit **312** for precharging local data lines LDL **305** and *LDL **307**. Having a precharge and equalization circuit **312** on the opposite side of isolation transistors **306** and **308** from the bit lines allows for a sense amplifier **314** of sense amplifier circuit **213** to be precharged while cells of bitcell array **203** are being written during a write cycle.

Sense amplifier **314** includes a pair of cross coupled inverters **318** and **320**. Inverter **318** is formed from transis-

tors **317** and **319** and inverter **320** is formed from transistors **315** and **321**. Transistors **319** and **321** each include a current electrode connected to a current electrode of transistor **323**. Transistor **323** receives the SENSE ENABLE signal at its control electrode. Sense amplifier **314** amplifies the difference in voltage between the local data lines LDL **305** and *LDL **307** in response to the assertion of the SENSE ENABLE signal. In one embodiment, when the SENSE ENABLE signal is asserted, sense amplifier **314** senses which of the local data lines (LDL **305** or *LDL **307**) has the lower voltage due to a differential data signal from a selected bitcell of array **203** via the bit lines and transistors **306** and **308**. Sense amplifier **314** then drives that local data line to a voltage of power supply terminal VSS and drives the other local data line to the voltage of the power supply terminal VDD to provide an amplified differential data signal.

In the embodiment shown, sense amplifier circuit **213** also includes buffers (e.g. inverters **327** and **325**) for isolating sense amplifier **314** from self-timed latch **215**. In other embodiments, sense amplifier circuit **213** does not include buffers. In still other embodiments, non inverting buffers may be utilized in place of inverters **327** and **325**.

Self-timed latch **215** includes transistors **337** and **335** whose control electrodes are connected to data lines DL **311** and *DL **313**, respectively. Transistors **337** and **335** each include a current terminal coupled to cross coupled inverters **331** and **333**. Self-timed latch **215** outputs data at its output, which is connected to the output terminal of inverter **331** and the input terminal of inverter **333**. Self-timed latch **215** provides at its output (DATA OUT) a value that corresponds to the value of the amplified differential data signal received on differential data lines DL **311** and *DL **313** in response to receiving the amplified differential data signal.

FIG. **4** shows one embodiment of a timing diagram for the circuit of FIG. **3** during two read cycles. The portion of the timing diagram labeled READ "1" CYCLE indicates the voltage values of various nodes, signals, and data lines during a read cycle of a selected memory cell of bit array **203** having a stored logic state indicative of a value of "1". The portion of the timing diagram labeled READ "0" CYCLE indicates the voltage values of various nodes, signals, and data lines during a read cycle of a selected memory cell of bit array **203** having a stored logic state indicative of a value of "0". The designation of a stored logic state to a value is arbitrary in that with some embodiments, the logic state of a memory cell that designates a "1" may designate a "0" in other embodiments. The CLOCK signal is provided by clock circuitry (e.g. **511** of FIG. **5**) external to the memory device.

During a read cycle, the CD signal is driven low (e.g. at **405**) to couple the local data lines LDL **305** and *LDL **307** to bit lines BL **205** and *BL **207**, respectively. During this time, a memory cell in bitcell array **203** is selected for reading by activating the word line (e.g. **210**) associated with that bitcell. Also when the CD signal is driven low, the PRECHARGE signal is driven high to deactivate the precharge of local data lines LDL **305** and *LDL **307** by precharge and equalization circuit **312**. Coupling the local data lines LDL **305** and *LDL **307** to bit lines BL **205** and *BL **207**, respectively, and deactivating the precharge and equalization circuit **312** allows the local data lines LDL **305** and *LDL **307** to be coupled to the selected bitcell to develop a voltage differential across LDL **305** and *LDL **307** that is dependent upon the logic state stored in the selected memory cell. For the embodiment shown, because a logic state designating a "1" is stored in the selected memory cell, the voltage of *LDL **307** is pulled to a lower voltage level (see sloped line **406**) than that of the voltage level of LDL **305** with the assertion of the CD signal.

After a predetermined period of time from when the CD signal is driven low at **405**, the SENSE ENABLE signal is asserted (the SENSE ENABLE signal is an active high signal) at **407**. The SENSE ENABLE signal, as well as the CD signal and the PRECHARGE signal, are logically derived from the CLOCK signal. Asserting the SENSE ENABLE signal triggers sense amplifier **314** to drive *LDL **307** to a voltage level of power supply voltage terminal VSS. At about the time that the SENSE ENABLE signal is asserted, the CD signal is driven high to isolate the local data lines LDL **305** and *LDL **307** from bit lines BL **205** and *BL **207**, respectively. Isolating the local data lines (e.g. LDL **305** and *LDL **307**) from the bit lines (BL **205** and *BL **207**) may allow for sense amplifier **314** to amplify the differential data signal on the local data lines faster than if they were coupled to the bit lines, in that the capacitance on the local data lines is reduced when they are not coupled to the bit lines.

Because *LDL **307** is connected to the input terminal of inverter **325** and data line *DL **313** is connected to the output terminal of inverter **325**, pulling *LDL **307** to VSS drives *DL **313** high. Because DL **311** is coupled to LDL **305** through inverter **327**, DL **311** remains at a low voltage level. In response to *DL **313** going to a high level to indicate that a "1" is stored in the selected memory cell, the DATA OUT signal transitions to a low state. DL *313 going to a high level makes transistor **335** conductive, over powering inverter **331** and pulling the input terminal of inverter **333** low. In response to the input terminal of inverter **333** being pull low, the input terminal of inverter **331** (node **341**) is pull high, thereby pulling the DATA OUT signal low.

When the SENSE ENABLE signal is deasserted and precharge and equalization circuit **312** is enabled by the PRECHARGE signal going low, local data line *LDL **307** is pulled back to VDD, thereby pulling *DL **313** low, which turns off transistor **335**. However, because of the latch function of self-timed latch **215**, the voltage level of the DATA OUT signal remains latched at the low voltage level. Accordingly, self-timed latch **215** provides a value indicative of the contents of the selected memory cell after the local data lines and sense amplifier **314** are being precharged.

The value of the DATA OUT signal remains at same level indicating a value until an opposite value is sensed by the sense amplifier during a subsequent memory read cycle. For example, the voltage of the DATA OUT signal remains at a low level until a "0" value is sensed by sense amplifier **314** during a subsequent memory read cycle.

During the READ "0" CYCLE, the CD signal is driven low (e.g. at **408**) to couple local data lines LDL **305** and *LDL **307** to bit lines BL **205** and *BL **207**, respectively. During this time, a memory cell in bitcell array **203** is selected for reading by activating the word line (e.g. **210**) associated with that bitcell. Also when the CD signal is driven low, the PRECHARGE signal is driven high to deactivate the precharge of local data lines LDL **305** and *LDL **307** by precharge and equalization circuit **312**. Because a "0" is stored in the selected memory cell, the voltage of LDL **305** is pulled to a lower voltage level than that of the voltage level of *LDL **307** (see sloped line **412** in FIG. **4**).

After a predetermined period of time from when the CD signal is driven low at **408**, the SENSE ENABLE signal is asserted at **409**. Asserting the SENSE ENABLE signal triggers sense amplifier **314** to drive LDL **305** to the voltage level of power supply voltage terminal VSS. At about the time that the SENSE ENABLE signal is asserted, the CD

signal is driven high to isolate the local data lines LDL **305** and *LDL **307** from bit lines BL **205** and *BL **207**, respectively.

Because LDL **305** is connected to the input terminal of inverter **327** and data line DL **311** is connected to the output terminal of inverter **327**, pulling LDL **305** to VSS drives DL **311** high. Because *DL **313** is coupled to *LDL **307** through inverter **325**, *DL **313** remains at a low voltage level. In response to DL **311** going to a high level to indicate that a "0" is stored in the selected memory cell, the DATA OUT signal transitions to a high voltage level. DL **311** going to a high voltage level makes transistor **337** conductive, over powering inverter **333** and pulling the input terminal (node **341**) of inverter **331** low. In response to the input terminal of inverter **331** being pulled low, the input terminal of inverter **333** and the DATA OUT signal are pulled to a high voltage level.

When the SENSE ENABLE signal is deasserted and precharge and equalization circuit **312** is enabled by the PRECHARGE signal going low, local data line LDL **305** is pulled back to VDD, thereby pulling DL **311** low, which turns off transistor **337**. However, because of the latch function of self-timed latch **215**, the voltage level of the DATA OUT signal remains latched at the high voltage level.

Providing a self-timed latch that is responsive only to the output of a sense amplifier circuit may allow for the latch to latch a value immediately after the sense amplifier provides an amplified data signal as opposed to a clocked latch which has specific setup and hold time requirements to be maintained in order to capture and retain the data of the amplified data signal. Also, providing a self-timed latch that does not have a clock input may allow for reduction in the load of the clock generating circuitry of an integrated circuit. It also may allow for a reduction in the circuitry to implement a latch and sense amplifier circuit in a memory device.

In other embodiments, the sense amplifier circuit and latch may have other configurations. For example, inverters **325** and **327** (which perform an inverting buffer function) may be replaced by non inverting buffers. In such an embodiment, transistors **337** and **335** would be replaced with P channel transistors and their current terminals would be connected power supply terminal VDD instead of VSS. Also in other embodiments, isolating transistors **306** and **308** may be removed. In other embodiments, other types of sense amplifier circuits maybe utilized including e.g. other sense amplifiers that provide an amplified differential output.

FIG. **5** is a block diagram of one embodiment of an integrated circuit according to the present invention. Integrated circuit **501** includes a core processor **503**, clock circuitry **511**, bus controller and direct memory access circuitry **505**, and an L2 cache **509**. In one embodiment, bus controller and direct memory access circuitry **505** includes one or more bus controllers, with each bus controller coupled to a different system bus (such as e.g. a PCI bus). L2 cache **509** includes a plurality of columns, with each including a sense amplifier circuit, self timing latch, and circuit portion similar to sense amplifier circuit **213**, self-timing latch **215**, and circuit potion **309** of FIG. **3**. Clock circuitry **511** provides a clock signal. Core processor **503** provides row and column address to L2 cache **509** via bus **515** and receives data from L2 cache **509** via bus **515**. Integrated circuit **501** may also include other devices such as other bus controllers and memories (e.g. RAM or Flash). In one embodiment, integrated circuit **501** is a communications processing circuit for operably coupling busses of different protocols.

In other embodiments, the sense amplifier circuit self-timed latch and column logic described herein may be used in other types of memory devices. For example, these circuits may be used in embedded memory circuits (e.g. embedded RAM or ROM) or in stand alone memory devices.

In one aspect of the invention, a memory device includes a plurality of memory cells. Each of the plurality of memory cells is coupled to a bit line. The memory device also includes a sense amplifier for amplifying a data signal from a selected one of the plurality of memory cells via the bit line to provide an amplified data signal in response to asserting a sense enable signal. The memory device further includes an isolation circuit coupled between the bit line and the sense amplifier. The isolation circuit is for decoupling the selected one of the plurality of memory cells from the sense amplifier at about the same time as the assertion of the sense enable signal. The memory device also includes a self-timed storage device, coupled to the sense amplifier, for storing data corresponding to the amplified data signal only in response to the amplified data signal.

In another aspect of the invention, a memory device includes a plurality of memory cells. Each of the plurality of memory cells is coupled to a first bit line and to a second bit line. The memory device includes a first data line coupled to the first bit line during at least a portion of a read cycle and a second data line coupled to the second bit line during at least a portion of the read cycle. The memory device further includes a sense amplifier having a pair of cross-coupled inverters. The pair of cross-coupled inverters is coupled to the first data line and to the second data line for amplifying a data signal from a selected one of the plurality of memory cells in response to asserting a sense enable signal. The memory device also includes a first buffer circuit having an input coupled to the first data line and an output, a second buffer circuit having an input coupled to the second data line and an output, and a self-timed storage device having a first input coupled to the output of the first buffer circuit and a second input coupled to the output of the second buffer circuit. The self-timed storage device is responsive only to a differential voltage between the output of the first buffer circuit and the output of the second buffer circuit.

In another aspect, the invention includes a method for reading a memory cell of a memory device. The memory device includes a plurality of memory cells. Each of the plurality of memory cells is coupled to a bit line and to a word line. The method includes selecting at least one of the plurality of memory cells and sensing and amplifying a voltage on the bit line using a sense amplifier in response to asserting a sense enable signal to produce an amplified data signal. The amplified data signal is representative of a logic state stored in the at least one of the plurality of memory cells selected by the selecting. The method also includes decoupling the bit line from the sense amplifier at about the same time as the sense enable signal is asserted and latching data corresponding to the amplified data signal in a self-timed latch. The self-timed latch latching the data in response to only the amplified data signal.

While particular embodiments of the present invention have been shown and described, it will be recognized to those skilled in the art that, based upon the teachings herein, further changes and modifications may be made without departing from this invention and its broader aspects, and thus, the appended claims are to encompass within their scope all such changes and modifications as are within the true spirit and scope of this invention.

What is claimed is:

1. A memory device, comprising:

a plurality of memory cells, each of the plurality of memory cells coupled to a bit line;

a sense amplifier for amplifying a data signal from a selected one of the plurality of memory cells via the bit line to provide an amplified data signal in response to asserting a sense enable signal;

an isolation circuit, coupled between the bit line and the sense amplifier, the isolation circuit for decoupling the selected one of the plurality of memory cells from the sense amplifier at about the same time as the assertion of the sense enable signal; and

a self-timed storage device, coupled to the sense amplifier, for storing data corresponding to the amplified data signal only in response to the amplified data signal.

2. The memory device of claim 1, wherein the memory device is implemented on an integrated circuit.

3. The memory device of claim 1, wherein the memory device is characterized as being a static random access memory (SRAM).

4. The memory device of claim 1, wherein:

the data signal is a differential data signal;

the amplified data signal is an amplified differential data signal;

the sense amplifier comprises a pair of cross-coupled inverters, the pair of cross-coupled inverters being coupled to amplify the differential data signal to provide the amplified differential data signal in response to the sense enable signal.

5. The memory device of claim 1, wherein the self-timed storage device comprises:

a first transistor having a first current electrode, a second current electrode coupled to a power supply voltage terminal, and a control electrode coupled to a first data line;

a second transistor having a first current electrode, a second current electrode coupled to the power supply voltage terminal, and a control electrode coupled to a second data line;

a first inverter having an input coupled to the first current electrode of the first transistor, and an output coupled to the first current electrode of the second transistor; and

a second inverter having an input coupled to the first current electrode of the second transistor and an output coupled to the first current electrode of the first transistor.

6. The memory device of claim 1, wherein the sense amplifier comprises:

a first transistor having a first current electrode coupled to a first power supply voltage terminal, a second current electrode coupled to a first data line, and a control electrode;

a second transistor having a first current electrode coupled to the second current electrode of the first transistor, a second current electrode, and a control electrode coupled to the control electrode of the first transistor;

a third transistor having a first current electrode coupled to the first power supply voltage terminal, a second current electrode coupled to the control electrode of the first transistor and to a second data line, and a control electrode coupled to the second current electrode of the first transistor;

a fourth transistor having a first current electrode coupled to the second current electrode of the third transistor, a second current electrode, and a control electrode coupled to the control electrode of the third transistor; and

a fifth transistor having a first current electrode coupled to the second current electrodes of both the second and fourth transistors, a second current electrode coupled to a second power supply voltage terminal, and a control electrode for receiving the sense enable signal.

7. The memory device of claim 1, wherein the data signal is a differential data signal provided on a first bit line and a second bit line, and the isolation circuit further comprising:

a first isolation transistor for selectively coupling the first bit line to a first data line; and

a second isolation transistor for selectively coupling the second bit line to a second data line.

8. The memory device of claim 7 wherein the sense amplifier is coupled to the first data line and the second data line, the first isolation transistor for selectively coupling the first bit line to the sense amplifier, the second isolation transistor for selectively coupling the second bit line to the sense amplifier.

9. The memory device of claim 7, further comprising:

a precharge circuit coupled to the first and second data lines, the precharge circuit for precharging the first and second data lines prior to the assertion of the sense enable signal.

10. The memory device of claim 7, further comprising:

a first inverter having an input coupled to the first data line and an output coupled to a first input of the self-timed storage device;

a second inverter having an input coupled to the second data line and an output coupled to a second input of the self-timed storage device.

11. The memory device of claim 10, wherein the self-timed storage device comprises:

a first transistor having a first current electrode, a second current electrode coupled to a power supply voltage terminal, and a control electrode coupled to the first data line;

a second transistor having a first current electrode, a second current electrode coupled to the power supply voltage terminal, and a control electrode coupled to the second data line;

a first inverter having an input coupled to the first current electrode of the first transistor, and an output coupled to the first current electrode of the second transistor; and

a second inverter having an input coupled to the first current electrode of the second transistor and an output coupled to the first current electrode of the first transistor.

12. A memory device comprising:

a plurality of memory cells, each of the plurality of memory cells coupled to a first bit line and to a second bit line;

a first data line coupled to the first bit line during at least a portion of a read cycle;

a second data line coupled to the second bit line during at least a portion of the read cycle;

a sense amplifier having a pair of cross-coupled inverters, the pair of cross-coupled inverters being coupled to the first data line and to the second data line for amplifying a data signal from a selected one of the plurality of memory cells in response to asserting a sense enable signal;

a first buffer circuit having an input coupled to the first data line and an output;

a second buffer circuit having an input coupled to the second data line and an output;

a self-timed storage device having a first input coupled to the output of the first buffer circuit and a second input coupled to the output of the second buffer circuit, the self-timed storage device responsive only to a differential voltage between the output of the first buffer circuit and the output of the second buffer circuit.

13. The memory device of claim **12**, wherein the plurality of memory cells is characterized as being a plurality of static random access memory (SRAM) cells.

14. The memory device of claim **12**, wherein the memory device is part of an integrated circuit.

15. The memory device of claim **12**, further comprising:

a first isolation transistor for selectively coupling the first bit line to the first data line; and

a second isolation transistor for selectively coupling the second bit line to the second data line.

16. The memory device of claim **15**, wherein the first and second isolation transistors decouple the first and second data lines from the first and second bit lines at about the same time as the assertion of the sense enable signal.

17. The memory device of claim **12**, wherein the sense amplifier comprises:

a first transistor having a first current electrode coupled to a first power supply voltage terminal, a second current electrode coupled to the first data line, and a control electrode;

a second transistor having a first current electrode coupled to the second current electrode of the first transistor, a second current electrode, and a control electrode coupled to the control electrode of the first transistor;

a third transistor having a first current electrode coupled to the first power supply voltage terminal, a second current electrode coupled to the control electrode of the first transistor and to the second data line, and a control electrode coupled to the second current electrode of the first transistor;

a fourth transistor having a first current electrode coupled to the second current electrode of the third transistor, a second current electrode, and a control electrode coupled to the control electrode of the third transistor; and

a fifth transistor having a first current electrode coupled to the second current electrodes of both the second and fourth transistors, a second current electrode coupled to a second power supply voltage terminal, and a control electrode for receiving the sense enable signal.

18. The memory device of claim **12**, wherein the self-timed storage device comprises:

a first transistor having a first current electrode, a second current electrode coupled to a power supply voltage terminal, and a control electrode coupled to the first data line;

a second transistor having a first current electrode, a second current electrode coupled to the power supply voltage terminal, and a control electrode coupled to the second data line;

a first inverter having an input coupled to the first current electrode of the first transistor, and an output coupled to the first current electrode of the second transistor; and

a second inverter having an input coupled to the first current electrode of the second transistor and an output coupled to the first current electrode of the first transistor.

19. The memory device of claim **12**, wherein the first and second buffer circuits are first and second inverters, respectively.

20. The memory device of claim **12**, further comprising a precharge circuit coupled to the first and second data lines, the precharge circuit for precharging the first and second data lines prior to the assertion of the sense enable signal.

21. The memory device of claim **12**, wherein the sense enable signal is generated from a clock signal.

22. A method for reading a memory cell of a memory device, the memory device comprising a plurality of memory cells, each of the plurality of memory cells coupled to a bit line and to a word line, the method comprising:

selecting at least one of the plurality of memory cells;

sensing and amplifying a voltage on the bit line using a sense amplifier in response to asserting a sense enable signal to produce an amplified data signal, the amplified data signal representative of a logic state stored in the at least one of the plurality of memory cells selected by the selecting;

decoupling the bit line from the sense amplifier at about the same time as the sense enable signal is asserted; and

latching data corresponding to the amplified data signal in a self-timed latch, the self-timed latch latching the data in response to only the amplified data signal.

23. The method of claim **22**, wherein the memory device is characterized as being a static random access memory (SRAM).

24. The method of claim **22**, wherein the sense enable signal is generated from a clock signal.

25. The method of claim **22** wherein the amplified data signal is produced on a data line, the method further comprising precharging the data line prior to the assertion of the sense enable signal.

26. The method of claim **22** further comprising:

prior to the sensing and amplifying, coupling the bit line to a data line wherein, the

coupling includes coupling the sense amplifier to the bit line via the data line;

wherein the amplified data signal is produced on the data line;

wherein the decoupling the bit line from the sense amplifier includes decoupling the bit line from the data line.

27. The method of claim **22** wherein the data remains latched until an other amplified data signal representative of an opposite logic state to the logic state is produced using the sense amplifier during a memory read cycle subsequent to the sensing and amplifying.

28. The method of claim **22** wherein:

the sensing and amplifying a voltage includes sensing and amplifying a differential voltage;

the amplified data signal is an amplified differential data signal.

29. A method for reading a memory cell of a memory device, the memory device comprising a plurality of memory cells, the method comprising:

selecting at least one of the plurality of memory cells;

sensing and amplifying a voltage using a sense amplifier in response to asserting a sense enable signal to produce an amplified data signal on a line, the amplified data signal representative of a logic state stored in the at least one of the plurality of memory cells selected by the selecting;

latching data corresponding to the amplified data signal in a self-timed latch, the self-timed latch latching the data in response to only the amplified data signal;

precharging the line after the sensing and amplifying, wherein the data remains latched at least during an initial portion of the precharging.

30. The method of claim **29** wherein the data remains latched until an other amplified data signal representative of an opposite logic state to the logic state is produced on the line during a memory read cycle subsequent to the sensing and amplifying.

31. The method of claim **29** wherein:

the sensing and amplifying a voltage includes sensing and amplifying a differential voltage;

the amplified data signal is an amplified differential data signal.

32. The method of claim **29**, wherein the memory device is characterized as being a static random access memory (SRAM).

* * * * *